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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,743	KANAI ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11,12 and 17-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,12 and 17-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 23, 2004 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5, 8, 11, 17-18, 22-23 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) in view of Dahlberg (USPN: 5,664,169). Regarding claims 1, 17-18 and 22, Tanabe discloses an information processing system (Figure 4) comprising a processor (Figure 4, Reference 3); a memory (Figure 4, Reference 5); a memory controller (Figure 4, Reference 1); a system bus connecting the processor and the memory controller (comprised of BC, A, D, BS in Figure 4); and a memory bus (RB) connecting the memory controller and the memory, the memory bus transferring an instruction code and data (Figure 4, RB), wherein the memory controller comprises a buffer (Figure 4, Reference 29R), a control circuit (Figure 4, comprised of References 21 and 23), an access judging circuit (Figure 4, Reference 30), wherein the control circuit estimates a most probable address to be accessed

next in the memory (C 10, L 19-50), and wherein the access judging circuit prefetches data [instruction code] stored in the most probable address of the memory, via the memory bus, into the buffer memory before a memory access is carried out from the processor (C 7, L 32-46; C 10, L 19-50 - the access judging circuit accesses the memory and thus performs the prefetching operation in response to a read request from the prefetch request unit which is performed before a memory access is carried out from the processor). Tanabe does not explicitly disclose at least two memory buses connecting the memory controller and the memory, the at least two memory buses comprising a first memory bus for transferring an instruction code from the memory to the processor to be executed by the processor and a second memory bus for transferring operand data from the memory to processor to be processed by the processor during execution of instructions codes. However, Dahlberg teaches the concept of two memory buses (Harvard bus architecture/ data bus and an address bus) comprising a first memory bus for transferring an instruction code from the memory to the processor to be executed by the processor and a second memory bus for transferring operand data from the memory to processor to be processed by the processor during execution of instructions codes (C 2, L 47-55; C 8, L 7-10). This feature taught by Dahlberg provides simultaneous access to data and instruction codes, which improves the latency and the performance of the system (C 2, L 53-55). In the system taught by Tanabe, the control information and data are multiplexed on the same bus, which increases the latency. Hence, it would have been obvious to one of ordinary skill in the art to modify Tanabe's system with two memory buses as cited above for the desirable purpose of improved performance by minimizing latency.

Regarding claims 5 and 23, Tanabe discloses a plurality of buffers into which prefetched data is stored and wherein the control circuit transfers data in the buffer memories to the processor in an order different from an address order (sequentially) (Figure 17, References 38A-38D; C 13, L 51-55; C 16, L 50-53; each memory is accessed independently (in any order), thereby providing non-sequential data access).

Regarding claims 8 and 26 Tanabe discloses the control circuit in its initial state (state during a first time processor access request) to prefetch data already stored at a pre-specified address (address specified by the first processor access) into the buffer (C 7, L 28-52 – 32 bytes of data are retrieved from the RDRAM into the prefetch buffer when a cache miss occurs wherein 16 bytes of the retrieved data are the requested data and the additional 16 bytes of data retrieved are the prefetched data).

Regarding claims 11 and 27, Tanabe discloses the processor comprising an internal cache (Figure 4, Reference 3a) and the control circuit is controlled to prefetch data having a data size of twice or more a line size of the internal cache (C 6, L 18-29; C 7, L 1-16). Tanabe discloses the line size of the internal cache as 16 bytes (C 5, L 26-28).

4. Claims 2 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) and Dahlberg (USPN: 5,664,169) as applied to claims 1 and 18 above and further in view of Genduso (USPN: 5,778,422).

Regarding claims 2 and 19-20, Tanabe and Dahlberg disclose control circuitry (Tanabe - Figure 4, References 21 and 23) controlled to transfer data to the processor, when the access from the processor hits data within the buffer (Tanabe - C 7, L 52-67; C 8, L 1-3). However, Tanabe and Dahlberg do not disclose a memory controller comprising a direct path (path excluding the buffer memory) for transmitting data directly to the processor from the memory there through, wherein the control circuit is controlled to transfer data within the memory to the processor via the direct path when the access from the processor fails to hit data within the buffer memory. However, Genduso does teach a memory controller comprising a direct path (Figure 1, Reference 18) for transmitting data directly to the processor from the memory there through; wherein the control circuit (C 5, L 27-30), is controlled to transfer the data to the processor when the access from the processor hits data within the buffer memory (Figure 4, References 80-82, 88-90; C 6, L 11-20, L 24-31), and wherein the control circuit is controlled to transfer data within the memory to the processor via the direct path when the access from the processor fails to hit data within the buffer memory (Figure 4, Reference 110, 112 and 108; C 6, L 49-60). One of ordinary skill in the art would have recognized the speed enhancement provided by transferring data to the processor from the memory controller via a direct path as taught by Genduso in comparison to the system taught by Tanabe and Johnson. In the system taught by Tanabe and Dahlberg the transferred data from the main memory is first stored in the buffer in the memory controller and then transferred to the processor from the buffer (C 7, L 40-52), which requires two data transfers instead of one, and additional control logic for managing both transfers and increased time. Therefore, it would have been obvious to one of ordinary skill in the art to use the teachings of

Genduso in the system taught by Tanabe and Dahlberg for the desirable purpose of improved performance and reduced latency.

5. Claim 3-4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) and Dahlberg (USPN: 5,664,169) as applied to claims 1 and 18 and further in view of Conary et al. (USPN: 5,935,253).

Regarding claims 3-4 and 21, Tanabe and Dahlberg discloses prefetching information, however, Tanabe and Dahlberg do not explicitly disclose prefetching instructions and data. However, Conary discloses prefetching instructions and data (C 4, L 61-65). It is common knowledge that prefetching is performed to provide fast access to information requested by the processor. Processors access instructions and data from memory in performing tasks and thus prefetching instructions and data would be desirable to provide prompt access to the instructions and data thereby reducing memory latency and improving the performance of the system. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to prefetch instructions and data in the system taught by Tanabe and Dahlberg for the desirable purpose of reduced memory latency and improved performance.

6. Claims 12 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) and Dahlberg (USPN: 5,664,169) as applied to claims 1 and 18 above and further in view of Genduso (USPN: 5,778,422), Lynch (USPN: 5,829,031) and Handy, The Cache Memory Book.

Regarding claims 12 and 28, Tanabe and Dahlberg disclose the limitations cited above in claims

1 and 18, additional, Tanabe and Dahlberg disclose, the memory divided into a first memory for storing therein an instruction code to be executed on the processor (Dahlberg portion of the memory storing instructions) and a second memory for storing therein operand data (Dahlberg – portion of the memory storing data) (C 4, L 33-35). However, Tanabe and Dahlberg do not disclose the memory controller comprising an access judgment circuit for judging whether the access from the processor is an access to the first memory or an access to the second memory, a first buffer memory for prefetching the instruction code and a second memory for prefetching of the operand data; wherein the control circuit is controlled to prefetch the instruction code into the first buffer memory according to a judgment of the access judgment circuit or to prefetch the operand data into the second buffer memory. However, Lynch discloses dividing a memory into a first memory for storing instructions (instruction cache) (Figure 1, Reference 22) and a second memory for storing operand data (data cache)(Figure 1, Reference 24), wherein a memory controller (Figure 1, Reference 20 and cache controller, not shown – inherent, determines cache hit/miss) has an access judgment circuit (Figure 1, Reference 20) for judging whether the access from the processor is an access to the first memory or an access to the second memory (C 6, L 47-56). Handy teaches that this type of split cache (memory) architecture reduces thrashing, which improves the performance of the system, and is simple to construct (Page 60-61, Section titled Unified vs. Split Caches). Furthermore, this configuration is known in the art as a Harvard architecture, which improves the bandwidth of the system, when the memories are accessed independently by providing parallel access to each memory unit. Additionally, Genduso teaches the concept of a first buffer memory for prefetching instructions (Figure 2, Reference 44), a second buffer memory for prefetching data (Figure 2, Reference 46)

and a controller (Figure 2, Reference 52) for prefetching instructions into the first buffer memory according to a judgment of an access judgment circuit (the circuitry/logic portion in the controller, which determines whether a processor access is an instruction request or a data request, Figure 3, C 5, L 36-67; C 6, L 1-64) or to prefetch data into the second buffer memory (C 8, L 51-67; C 9, L 1-67; C 10, L 1-7). As stated above, prefetching instructions and data improves the performance of the system by providing prompt access to information requested by the processor, which includes instructions and data. The system taught by Tanabe and Dahlberg teaches the use of one prefetch buffer, which may be subjected to thrashing issues, depending on what type of information is stored in the prefetch buffer. It would also be desirable to implement a Harvard architecture memory structure in Tanabe's system to increase the storage capacity and the bandwidth of the memory system. Thus it would have been obvious to one of ordinary skill in the art to use the teachings of Lynch, Handy and Genduso with the system taught by Tanabe and Dahlberg for the desirable purpose of improved performance.

7. Claims 6 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) and Dahlberg (USPN: 5,664,169) as applied to claims 1 and 18 above and further in view of Suzuki (USPN: 5,381,532).

Tanabe and Dahlberg disclose the limitations cited above in claims 1 and 18, however, Tanabe and Dahlberg do not disclose the memory controller having an instruction decoder and a branching buffer, wherein the control circuit prefetches an instruction as a branch destination into the branching buffer when the instruction decoder detects a branch instruction and determining whether or not an instruction hits data within the buffer and the branching buffer

when an access is made from the processor to the instruction. However, Suzuki discloses a memory controller (comprised of Figure 1, References 110, 150; Figure 2, entire) having an instruction decoder (Figure 2, Reference 130) and a branching buffer (Figure 2, Reference 201), wherein the control circuit (Figure 1, Reference 150, Figure 2, References 200, 202 and 205) prefetches an instruction as a branch destination into the branching buffer when the instruction decoder detects a branch instruction (C 5, L 38-40, L 46-58) and when an access is made from the processor to the instruction (branch taken) determining whether or not the instruction hits data within the buffer or the branching buffer (C 6, L 10-20 – the output of VTAKEN and UTAKEN determine whether the instruction is in the buffer or the branching buffer, when VTAKEN is active, the branch decoder outputs a high on signal 2021 in Figure 2, which allows the output of the branch buffer through the multiplexer to the instruction decoder and when the output of UTAKEN is high the output of the prefetch buffer is sent to the instruction decoder - C 6, L 62-66). Suzuki teaches that the above features enhances prefetching and branch processing thereby improving the performance of the system (Abstract). Tanabe and Dahlberg teach prefetching instructions and data sequentially from the requested address. If the processor executes a branch instruction, it is likely that the next instruction executed is not sequential to the branch instruction, unless the branch isn't taken. Therefore, the prefetched instructions will not be useful. Thus, it would have been obvious to one of ordinary skill in the art to use the teachings of Suzuki with the teachings of Tanabe and Dahlberg for the desirable purpose of increasing the effectiveness of prefetching and improved performance.

8. Claims 7 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe

(USPN: 5,752,272) and Dahlberg (USPN: 5,664,169) as applied to claims 1 and 18 above and further in view of Mirza (USPN: 5,357,618).

Tanabe and Dahlberg disclose the limitations cited above in claims 1 and 18, however, Tanabe and Dahlberg do not explicitly disclose the memory controller comprising a register for instructing start (enable) or stop (disable) of prefetch to the buffer memory. However, Mirza teaches the concept of starting (enabling) or stopping (disabling) prefetch operations to a buffer via a register (C 2, L 60-68; C 3, L 5-12). Mirza teaches memory access patterns are not always sequential and in such cases when prefetching is performed for sequential accesses the prefetch buffer/cache becomes polluted with data never referenced (C 1, L 36-68; C 2, L 1-33). Mirza's technique of selectively enabling and disabling prefetch operations optimizes the performance of the system by preventing prefetching for data stored at non-sequential (non-loop) access locations to prevent polluting the cache to reduce the cache miss rate. The system taught by Tanabe and Johnson seeks to reduce the cache miss rate by prefetching (C 14, L 21-25). Tanabe teaches that the cache miss rate can be reduced by the success of prefetch. The prefetch is successful when referenced data (non-polluted) is retrieved via the prefetch operation. One of ordinary skill in the art at the time of the invention would have recognized the improved prefetch success rate afforded by Mirza's teachings and would have been motivated to use the teachings of Mirza with the teachings of Tanabe and Dahlberg for the desirable purpose of improving the success rate of the prefetch operations and improving the performance of the system by reducing the cache miss rate.

Response to Arguments

9. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M (10:00 - 6:30); Tues, Thr (10:00 - 4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

November 13, 2004